High Energy Time Domain Thermal Sensor for SOC Thermal Management

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Abstract: The thermal sensor is used for on chip thermal sensing. We recommend an every digital on chip/module stage based thermal detector for system on a module (SoC) heat management. For onmodule reason, the planned thermal detector achieves area-efficient also quick thermal monitoring by adopting an Unstable / Digital Controlled Oscillator (URO/DCO). Thermal mensuration results are provided through a time support value produce by a simple counter. Later, the correctness of the future thermal detector is able to enhance by little area also less power using up. This upcoming thermal sensor (detector) is able to simply mensuration by a suggestion pulse. Since the future temperature detector can be just calibrated with a reference clk. The power of the heat detector is 21.6751mw also the total area of the temperature detector is 669.487487 µm2.

Keywords: Thermal detector, one-point calibration, process deviation, Thermal management, low power.


1 Introduction
The plan is measuring thermal on Field Programmable Gate Arrays (FPGAs) without using any on board thermal detectors. Power sufferers are occurred by thermal since designing imperfection. The profit of digital detector enhanced than an analog detector is tiny module volume also power is used. This want for less sized, high precision modules has developed over time also stipulates for little exploitation thermal detector has also grown. Also, require also for these detectors to consume less power has grown as the desire to prevent internal over thermaling also get better battery existence has grown. Clientele on the other contain happen to extra concerned by the lessening exactness, or die amount when buying cheaper detectors. Recent technological focus has been in the direction of wholly digital detectors by utilized of a counter to make the digital output.

The hold off also progression distinction is inflated through the thermal in on module. While numerous pieces are included too made up on a solo slice, this power foolishness is typically better. So, definite area of the slice concerning steep switch behavior be able to generate a confine steep thermal region describe a thermal place.” The TDC is used to translate a hold off line into the thermal message. A thermal detector should take up a tiny slice region permit many detectors near exist located within circuit in favor of localize thermal capacity progression.

II. Previous Time Realm Thermal Detector
In this section, we talk about the universal thought of FPGAs also how thermal relates to proliferation hold off. FPGAs offer a large podium for this completion. FPGAs yields high act at comparatively low cost, consumes a comparatively little area, also typically especially is reprogrammable. In the the past, smart thermal detectors have been frequently constructing using ADC converters. ADCs explanation for a enormous module part, extra power spending, also commonly gets nearer by a controlled thermal range. In this project, TDC was use in place of the ADC converter. The TDC was common among a pulse maker to create a digital output. To solve this problem, the thermal detector adopting single point calibration was suggested. It requires mensuration result at simply one known thermal point but it shows compatible mensuration precision with thermal detectors with two-point calibration.

By the quick development of scientific also engineering, dissimilar kind of huge presentation with small rate structure created at this bazaar.

The, generally state-of-the-art industrial SoCs employ heat sensors. Since these state-of-the-art SoCs have a massive thermal slope over the chip due to the high integration and high working speed, many temperature sensors are used in a single SoC. To promptly handle the measured value from the numerous temperature sensors in an SoC, a high conversion rate of the heat sensor is necessary.
An ADC of in excess of 10 bits is typically essential to get the necessary thermal declaration on the cost of huge slice part also more energy utilization. Following calibration is total, when the signal “Start” is enabled, the start controller send the signal “Enable” to activate the main sensor circuit. The major sensor circuit measures the present heat message and outputs a digital code (TDC code) to the temperature calculator to calculate the temp value.

Earlier thermal detectors want to execute two thermal position menstruations by a set DC provide prior to this thermal detectors be able to exercise. Or else, the result of progression difference preserve powerfully pressures this precision of thermal capacity. A twin holdup safe circle based every multi level thermal detector is future to eliminate the effects of progression distinction by way of calibration at just single thermal location The calibration progression has to be executed in a stable ambient temperature surroundings. As a reference measurement a high sensitivity calibrated thermometer can be used with accuracy is greatest. It has to be ensured that the chip/module is not pre-heated with an extensive application execution. The measurement of the calibrated temperature Tcal is realized by measuring the chip/module surface temperature. This thermal detector should exist simply standardize lacking with some outer power reference. This detector to achieve each this need shall consistent with simple designate in favor of into circuit thermal sense. High thermal also thermal deviation cause dishonored consistency, slower devices, rising resistances also leaking power also presently.

Over fifty percentages of all integrated module failures are related to thermal issue. Since of such troubles, high thermal cause by forever increasing miniaturization also enhanced power densities in new generation of VLSI desire that thermal consideration be taken into account through plan, developed check at run time.

III. Working Information Also Design Considerations

A. Promulgation delay vs

Thermal Spread hold off is the quantity of time it takes for a logic gate to toggle to the exact output after any of its inputs contain distorted. Hold off of alter opening logic one to logic zero may be different from the hold off alter initial logic zero to logic one. As well, depending on the superiority of the machinery of the gates insincere, promulgation hold off might vary. Also, promulgation hold off may attribute to glitches in digital mechanism as logic block might not vary quicker than others resulting in an unpreserved output.

B. Calibration Mode

\[
D_{inv} = T \cdot \alpha \cdot P_{inv}
\]

Where, \( D_{inv} \) is the hold off of CMOS inverter, \( T \) is the total thermal, \( \alpha \) is a thermal coefficient that depends on the progression technology also \( P_{inv} \) is a progression only dependent term in the hold off of the inverter.

\[
PW_{URO \ out} = N_C \cdot T_C \cdot \alpha \cdot P_{cell}
\]

Where, \( N_C \) is the amount of activate hold off gates in the URO at \( T_C \). \( T_C \) is the calibration thermal also the \( P_{cell} \) is the progression only dependent term in the hold off of the delay cell.

C. Sensing Mode

\[
PW_{URO \ out} = N_o \cdot T_o \cdot \alpha \cdot P_{cell}
\]

Where \( N_o \) is the amount of activated hold off gates in the URO. \( T_o \) be the operating thermal also the \( P_{cell} \) is the progression only dependent term in the hold off of the URO gates. The outside pulse is applied to the hold off line also the hold off clk (CLK hold off) is generated. The hold off line generally consists of the set of CMOS gates. In this case, the hold off between CLK\_EXT also CLK\_hold\_off is dependent on the thermal deviation. The time-realm thermal detector measures the thermal by measuring the hold off between the CLK\_EXT also the CLK\_hold\_off. The future thermal detector using one point calibration also it consist five types of components like URO, counter, three regs (N-reg, T-reg, also R-reg), comparator, Digital/binary-to-thermometer converter (DTC/DTC), also down counter (DN-counter).
D. Temperature Mensuration Block

The temperature deviation detector measures the change in PWdco by apply CLK ref also CLK dco to the XNOR gate. The output of the temperature deviation detector (OUT tvd) has a pulse width that is the same as the distinction between the negative pulse widths of CLK ref also CLK dco. OUTtvd is gated with E, also thus, it is generated only in the mensuration mode. The mensuration counter is used to convert OUTTVd into VALUE TEM.

Fig 2 Temperature Mensuration Block

The stored k-bits are transmitting to the comparator when the hold off PWURO out toggles the T-reg. The N-reg consists of n-bit D-flip-flops also stores Binary in order to mensuration the thermal. The comparator compares thermal value with suggestion value.

The comparison result controls the DTC. If thermal value is not the similar as Reference value, then the comparator generates a high-pulse comparator out to activate the DTC with the DN-counter. Otherwise, the comparator generates a low-pulse comparator out to deactivate the DTC with the DN-counter.

The DTC converts Binary value to URO control of the thermometer value to correct the numeral of activated hold off cells in the URO. When Comparator out is high, the DN counter decrease Binary value.

A, Unstable Ring Oscillator

A URO is a chain of an amount of INVERSE AND gates whose output is linked reverse to the input. When adequately a lot of gates are used it is likely to build a close to square wave model. To implement changeable hold off cells in the URO, a hold off unit is used. The hold off unit is shown in Fig. 3. The output node of the last INVERSE AND gate is tied to the input node of the first INVERSE AND gate. The INVERSE AND gate hold off cells work as a URO during the high pulse width of the start signal. One hold off cell is made up of four INVERSES AND gates also one of which acts as a dummy INVERSE AND gate.

If URO control is all-low, all hold off cells are deactivated also the shortest PWURO out is generated. If URO control is all-high, all hold off cells are activated also the longest PWURO out is generated. The hold off of the INVERSE AND gates depends on the progression technology.

Fig 3 Block diagram of upcoming thermal detector

The reference thermal is determined by the Reference value also the period of the TCLK. The counter also T-reg counts the number of cycles of CLKCNT during PWURO out, also estimate the counted number with Reference value. The control bit of the URO is adjusted by the comparison results until Temp value equals to Ref value.
is coupled to the input joint of the first INVERSE AND gate, also thus, the INVERSE AND gate holdup line operate as a URO during the high pulse width of the start signal.

<table>
<thead>
<tr>
<th>Internal</th>
<th>Switching Power</th>
<th>Leakage Power</th>
<th>Total Power (%  )</th>
</tr>
</thead>
<tbody>
<tr>
<td>io_pad</td>
<td>0.0000</td>
<td>0.0000</td>
<td>0.0000 ( 0.00%)</td>
</tr>
<tr>
<td>memory</td>
<td>0.0000</td>
<td>0.0000</td>
<td>0.0000 ( 0.00%)</td>
</tr>
<tr>
<td>black_box</td>
<td>0.0000</td>
<td>0.0000</td>
<td>0.0000 ( 0.00%)</td>
</tr>
<tr>
<td>clk_network</td>
<td>0.0000</td>
<td>0.0000</td>
<td>0.0000 ( 0.00%)</td>
</tr>
<tr>
<td>reg</td>
<td>0.0000</td>
<td>0.0000</td>
<td>0.0000 ( 0.00%)</td>
</tr>
<tr>
<td>sequential</td>
<td>0.0000</td>
<td>0.0106</td>
<td>0.0163 ( 0.49%)</td>
</tr>
<tr>
<td>combinational</td>
<td>0.0000</td>
<td>21.1678</td>
<td>21.1678 ( 97.66%)</td>
</tr>
</tbody>
</table>

Total 0 mW 21.6751 mW 21.6751 mW

The model INVERSE ANDgate is used to maintain the fan-out of each INVERSE ANDgate. For the n-bit N-reg, the amount of changeable defer cell in a INVERSE ANDgate defer line is 2n, also hold off cells are in sequence activate by a 2n-bit thermometer value.

The production of the sequence would alter when the earlier output is upturned since of the odd amount of INVERSE ANDgates later than the gates promulgation defers. If URO con is all-low (all-high), all hold off cells are deactivated also the shortest PW URO out is generate. The hold off of the INVERSE ANDgates cannot be reduced much by increasing the size of INVERSE ANDgates. The hold off of the INVERSE ANDgates rather depends on the progression technology.

Wire Load Model Mode: enclosed

B. Thermal Deviation Detector

Fig 5 Power report from Synopsys

Fig 6 Timing Report from SYNOPSYs

Fig 7 Temperature deviation detector

Fig 8 Simulation result for Thermal detector while Sensing

Fig 9 Simulation result for Temperature Mensuration Block

Fig 8 Output for Thermal detector while calibration
V. Conclusion

Each indication are technique in time base in place of usual voltage or current area. On-module thermal detectors for SoC thermal managing are right now in require also.lacking using any full-custom cell circuit the future thermal detector make a clk hold off which is comparative to the mensuration thermal also transfer this hold off into a equivalent digital bits. The future thermal detector takes away the desire for two thermal spot calculations in past thermal detectors. Hence thermal detector calibration hard work can be noticeably abridged. The prospect plan uses proposal clk phase message which is used to perform auto calibration also thus belongings of process deviation can be detached.

References


